Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct typographical errors and to add a description of items 28A and 28B, shown in Figures 4 and 5 as required by Examiner.

The claims have been amended to clarify Applicants invention.

Support for the amended claims is found in the original claims and the Specification.

No new matter has been added.

For example support for the amendments is found in the Specification at paragraph 0020:

"The contact region 12 may be a **conductor contact region** (i.e., formed employing a conductor including but not limited to a metal, metal alloy, doped polysilicon (having a dopant concentration of from about 1E18 to about 1E22 dopant atoms per cubic centimeter) or metal silicide (doped polysilicon/metal

silicide stack)) conductor. Alternatively, the contact region 12 may be a semiconductor contact region formed employing a semiconductor material including but not limited to less highly doped silicon, germanium and silicon-germanium alloy semiconductor materials (i.e., from about 1E14 to about 1E16 dopant atoms per cubic centimeter)."

Claim Rejections under 35 USC 102

1. Claim 1-20 stand rejected under 35 USC Section 102(b) as being anticipated by Knall et al. (US 6,420,215).

Knall et al. disclose a multi-level memory array that uses "rail stacks" that are formed perpendicular to one another (see Abstract; Figure 1 (items 18, and 16). Knall et al. discloses a first rail stacks are formed on an insulator layer (12) where the rail stack includes a conductive layer (14) on the insulator layer (12) where the conductive layer is disclosed **may be a metal silicide** (col 3, lines 14-29) or aluminum or copper, or other metal alloys such as MoW, or highly doped semiconductor or TiN; followed by formation of a **highly doped semiconductor layer (15) on the conductor layer**, where the layer 15 is disclosed may be polysilicon (15), or other semiconductor (col 3, lines 30-36).

The conductor and semiconductor (doped polysilicon) layers are then etched (patterned) to form half rail stacks, followed by forming **an anti-fuse layer 20,** which is deposited over the half rail stacks **or** grown selectively on the upper surface of etched semiconductor layer (15), where the anti-fuse material is disclosed to be silicon dioxide, silicon nitride, silicon oxynitride, amorphous carbon, and other insulating materials and also teach that an undoped layer of polysilicon (col 3, lines 41-58) may be used as the anti-fuse layer. On top of the anti-fuse layer is formed a highly doped polysilicon layer (21) (opposite in polarity to layer 15) perpendicular to the fuse layer. **Thus, here the conductor layer which is disclosed to be metal silicide is formed on a doped semiconductor layer (15).**

In another embodiment (Figure 3), Knall et al. disclose an embodiment which shows three complete levels of the array where the rail stacks 4, 5,, and 6, sandwiched between anti-fuse layer materials (e.g., 51 and 42)) and a conductor layer (e.g., 46) sandwiched between a highly doped upper semiconductor layer and two doped lower semiconductor layers (44 and 45) (col 5, lines 35-49). In this case, the upper doped semiconductor layer, the

conductor layer, and the two lower conductor layers are all patterned (etched), whereas the anti-fuse layer is unpatterned.

In another embodiment (Figure 4), Knall et al. disclose forming **two doped semiconductor layers (81 and 82) on a conductor layer** (80) (col 7, lines 30-38), followed by **formation of an anti-fuse layer** (83)) and formation of a doped semiconductor layer (84) of opposite polarity than **semiconductor layers (81 and 82) on the anti-fuse layer (83)**; all of the above layers are then etched to form **patterned layers** (including the conductor layer (80).

Thus, Knall et al. fail to teach several aspects of Applicants disclosed and claimed invention including:

"An anti-fuse structure comprising:

a substrate having formed therein a **conductor contact region;**

a metal silicide layer formed over and electrically connected with the conductor contact region;

a first doped polysilicon layer formed upon the metal silicide layer;

an anti-fuse material layer formed upon the first doped polysilicon layer; and

a second doped polysilicon layer formed upon the anti-fuse material layer."

As noted above, Knall et al. disclose a conductor (which may be metal silicide) sandwiched between doped semiconductor layers (Figure 3), where a doped polysilicon layer (15) is formed on the conductor layer (14) (Fig 2), which is formed on an insulator (12) or where the conductor (31) is formed on a semiconductor layers (item 30); or Figure 4, where a conductor layer (85) is formed on a semiconductor layer (84).

Nowhere does Knall et al. teach **a metal silicide layer formed over and electrically connected with the conductor contact region.**

Thus, Knall et al. is insufficient to anticipate Applicants disclosed and claimed invention as to Applicants independent as well as Applicants dependent claims.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Conclusion

The claims have been amended to clarify Applicants disclosed and claimed invention.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in

a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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